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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,666	09/30/2003	Randy B. Osborne	42P16964	8981

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EXAMINER	
SCHLIE, PAUL W	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,666	OSBORNE, RANDY B.	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/19/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

Response to Arguments

2. Applicant's arguments filed 1/19/06 have been fully considered but they are not persuasive.

With respect to arguments pertaining to the rejection of claims 14-15 under 35 U.S.C. §112; as claim 14 clearly cites "carry out a test of a memory device to determine", and where as "test" strongly implies the use of a speculative method, not a deterministic query of a specifically designated memory location within a standardized EEPROM for this specific purpose (in which case it's use would have been correspondingly obvious), and no such method has been disclosed nor considered otherwise obvious, the claims are correspondingly not considered enabled.

With respect to the arguments cited pertaining to the rejection of claims 1-15 under 32 U.S.C. §103 relying on that considered to be acknowledged as obvious to those of ordinary skill in the art by Osborne (10/676,666); although the interpretation of that cited within paragraph [0026] may be considered an instant application of that taught by the disclosure of the invention itself, its interpretation as a clear antidotal acknowledgement of prior art is based solely on that previously acknowledged as prior art by Osborne within the "Background" section of the disclosure within which for example in paragraph [0002] it is further acknowledged that "It has also become common practice to attempt to reduce both costs and the physical size of DRAM devices by multiplexing multiple functions onto the various signal inputs and outputs",

thereby correspondingly clearly acknowledging as prior art that any arbitrary physical signal may be assigned any arbitrary logical role as a may be desired to achieve it's correspondingly acknowledged benefit, thereby not qualifying as an instant application of the disclosed invention.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 14-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As claims 14 (and 15 being dependant on 14), cites executable code causing the electronic device to "carry out a test of a memory device to determine whether or not the memory device supports ..." a particular set of attributes; however the method necessary to facilitate this is neither sufficiently detailed in the specification, nor sufficiently obvious to enable one of ordinary skill in the art to enable without undue experimentation and/or more specific disclosure of the intended method itself.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590) in further view of Osborne (US Application 10/676,666).

As per claims 1-4, Watanabe teaches a multi-bank memory comprised of memory cells organized into arrays of rows and columns, where only one row of memory cells may be activated to be accessible at a given time; coupled to control logic which controls accesses made to each bank in response to commands received from an external device including a pre-charge command; wherein the banks affected by the command may be individually specified, see figure 2; but does not explicitly teach that the naturally existing independent bank pre-charge enable signals as are depicted within the embodiment as may be analogously exposed at the interface boundary as other similar signals such as address lines have been (considered to be clearly resulting from a conscious decision to correspondingly depict the integration of pre-charge control logic within the example embodiment, not due to a lack of obviousness that this logic and corresponding independent bank pre-charge enable control signals may be analogously alternatively partitioned in a variety of ways). Correspondingly, Osborne acknowledges that "... those skilled in the art will readily recognize that any combination of address signal lines and/or other signal lines (perhaps control lines) may be employed for the purposes of specifying banks(s) affected by a given pre-charge command and/or providing interoperability with existing DDR variants ...", referring to Figure 2b, which similarly depicts bank pre-charge enable signals and functionality as

disclosed by Watanabe; see page 13, lines 16-19. Therefore it is considered obvious to one of ordinary skill in the art to enable independent memory bank pre-charge selection by alternatively exposing an independent discrete encoding of such a designation potentially multiplexed with other analogous signals in a variety of analogous ways potentially enabled in alternate forms through the use of conventional programmable configuration mode registers, for the benefit of enabling more direct external control over the signals and/or behavior naturally inherent within such a device as may be desired for any arbitrary purpose.

As per claim 5, where claim 2 is covered by Watanabe and Osborne above, Osborne teaches by acknowledgement the obviousness of the support of an auto-pre-charge command by citing "As will be familiar to those skilled in the art, a read or write command with auto-pre-charge (a pre-charge command embedded within the read or write command) causes a combination of a read or write operation immediately followed by a pre-charge operation to take place", see page 14 lines 1-2. Thereby it would be obvious to one of ordinary skill in the art to include support of an auto-pre-charge in the control logic of such a memory device, for the benefit of potentially improving the signaling efficiency of it's interface.

1. Claims 6-9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590) and Osborne (US Application 10/676,666), in further view of "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" second edition, as published 10/2002 in English, and 8/2002 in Japanese.

As per claims 6-9 and 11-13, Watanabe and Osborne teach a multi-bank memory comprised of memory cells organized into arrays of rows and columns, where only one row of memory cells may be activated to be accessible at a given time, coupled to control logic which controls accesses made to each bank in response to commands received from an external device including a pre-charge command wherein the banks affected by the command may be individually specified similarly to claims 1-5 above; however does not teach an external memory controller connected to a CPU and such a memory which may be configured by; where the memory controller further comprises employing at least one prediction algorithm to determine which row must be open in a memory bank in preparation for an upcoming predicted access command and transmitting either an explicit pre-charge command or an implicit pre-charge command to be carried out immediately proceeding that access command. "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" teaches such a memory controller connected to a CPU and memory as claimed, see pages 22 and 25. It would be obvious to one of ordinary skill in the art to combine a CPU and memory controller with such a memory for the benefit of enabling their interaction to enable the more efficient memory device access.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590), Osborne (US Application 10/676,666), and "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" in further view of Rovati (6,182,192).

As per claim 10, Watanabe, Osborne, and "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" teach claim 9, but does not teach that the upcoming access command may depend on the predicted state of the a block's line row pre-charge state, and a queue of outstanding memory access requests. Rovati teaches such a memory controller; see figure 3, and abstract lines 1-22. Therefore it would be obvious to one of ordinary skill in the art to combine the two for the benefit of potentially improving the memory transaction performance/efficiency of such a system.

8. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590), Osborne (US Application 10/676,666), and "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" in further view of Shaver et al. (5,974,501).

As per claims 14-15, Watanabe, Osborne, and "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" teach a controller coupled to both a CPU and memory device, capable of being configured by executable code which may exist on a machine accessible medium, to enable the use of a pre-charge command as similarly claimed in claims 1-5 above; but does not teach a method to test the type of memory present in such a system to determine it's mode(s) of operation, and thereby correspondingly the necessary programmable configuration of a controller to enable a particular mode's subsequent utilization. Shaver et al. teaches that executable code enables a system comprised of such components may test and determine supported modes of operation of such a memory device, and may be subsequently utilized to program the behavior of a controller to utilize that determined mode of operation; see

figure 6, and column 1 lines 1-2. It would be obvious to one of ordinary skill in the art to combine the ability to dynamically determine the attributes of the memory devices interconnected to a memory controller for the benefit of being able to more flexibly and efficiently support a broader range of memory devices within a given system.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765, and email is [paul.schlie@uspto.gov]. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
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